UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,424	04/18/2006	Moriyoshi Nakashima	KOMOP0113US	9229

43076 7590 05/30/2008

MARK D. SARALINO (GENERAL)
RENNER, OTTO, BOISSELLE & SKLAR, LLP
1621 EUCLID AVENUE, NINETEENTH FLOOR
CLEVELAND, OH 44115-2191

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

MAIL DATE	DELIVERY MODE
05/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,424	NAKASHIMA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1,7,8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/6/07; 4/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/595424 Attorney's Docket #: KOMOP0113US
Filing Date: 4/18/2006; claimed foreign priority to 10/20/2003

Applicant: Nakashima et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1, 7 11 and 12), filed 3/4/2008, has been acknowledged.

This application contains claims 8 and 10 drawn to an invention non-elected without traverse

Claims 2-6 and 9 have been cancelled.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claims 1, 7 and 11, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1, 7, 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram (U.S. Patent Application Publication # 2007/0278648 A1).

1. Akram (figures 1 to 10) specifically figure 5 show a semiconductor device comprising: a substrate-like **27** or frame-like base material on which a plurality of semiconductor chips are mounted, wherein a semiconductor chip **(chip on large 27,26 on the left side)** mounted interposer **(26 on that chip on the left side)** configured by mounting a semiconductor bare chip on an interposer in which inside terminals to which terminals of the mounted semiconductor bare chip are connected, outside terminals to which terminals other than the terminals of the semiconductor bare chip are connected, testing terminals to

which testing electrodes of a testing apparatus are connected, and conductive wiring that makes an electrical connection between the inside terminals, the outside terminals and the testing terminals, are formed, and detaching the testing terminals after predetermined reliability testing or operation testing wherein the semiconductor chip mounted interposer is mounted along with another semiconductor chip **24** to the base material, and the semiconductor chip mounted interposer and the other semiconductor chip are resin sealed **(see figure 7**) along with the base material.

7. Akram (figures 1 to 10) specifically figure 5 show a semiconductor chip **(chip on large 27,26 on the left side)** mounted interposer **(26 on that chip on the left side)**, configured by mounting a semiconductor bare chip on an interposer in which inside terminals to which terminals of the mounted semiconductor bare chip are connected, outside terminals to which terminals other than the terminals of the semiconductor bare chip are connected, testing terminals to which testing electrodes of a testing apparatus are connected, and conductive wiring that makes an electrical connection between the inside terminals, the outside terminals and the testing terminals, are formed, and detaching the testing terminals after predetermined reliability testing or operation testing.

11. Akram (figures 1 to 10) specifically figure 5 show a bare chip **(chip on large 27,26 on the left side)** mounted interposer **(26 on that chip on the left side)**, in which: inside terminals to which terminals of a mounted semiconductor bare chip are

connected, outside terminals to which terminals other than the terminals of the semiconductor bare chip are connected, testing terminals for connecting testing electrodes of a testing apparatus, formed on the outer side of the inside terminals and the outside terminals, with a larger pitch than the inside terminals and the outside terminals, and conductive wiring that makes an electrical connection between the outside terminals, the inside terminals, and the testing terminals, are formed.

12. An interposer sheet configured by joining a plurality of the interposers according to claim 11, Akram show in a single body in the form of a matrix.

As to the grounds of rejection under section 103, see MPEP § 2113.

The listed references are cited as of interest to this application, but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

6/1/2008

/Alexander O Williams/
Primary Examiner, Art Unit 2826